ABSTRACT OF THE DISCLOSURE

A synchronous transmission module is disclosed, including a UTOPIA interface chip for transmitting UTOPIA level-2 data. A pair of STM interface chips receive UTOPIA level-1 data. A UTOPIA memory converts UTOPIA level-2 data into UTOPIA level-1 data and transfers the UTOPIA level-1 data to one of the pair of STM interface chips, according to a transmission address. A UTOPIA interface control part converts the transmission address, depending on states of the STM interface chips. Therefore, variable duplexing of the plurality of STM interface chips in a board is made possible.